Notice of References Cited

Application/Control No. 10/808,288	Applicant(s)/Patent Under Reexamination MALEVILLE ET AL.		
Examiner	Art Unit		
Stanetta D. Isaac	2812	Page 1 of 1	

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	Α	US-5,727,578	03-1998	Matthews, Robert Roger	134/61
	В	US-6,124,210	09-2000	Chino et al.	438/706
	С	US-5,911,837	06-1999	Matthews, Robert Roger	134/2
	D	US-5,776,296	07-1998	Matthews, Robert Roger	156/345.11
	E	US-6,239,045	05-2001	Tanaka et al.	438/507
	F	US-6,240,933	06-2001	Bergman, Eric J.	134/1.3
	G	US-6,273,108	08-2001	Bergman et al.	134/102.1
	Н	US-6,591,845	07-2003	Bergman et al.	134/100.1
	1	US-6,689,284	02-2004	Nakasaki, Yasushi	216/64
	J	US-6,849,192	02-2005	Nakasaki, Yasushi	216/64
	к	US-2001/0027799	10-2001	Bergman, Eric J.	134/3
	L	US-2002/0020436	02-2002	Bergman, Eric J.	134/30
	М	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	Z					
	0					
	Р					
	Ø					
	R					
	S					
	Т					

NON-PATENT DOCUMENTS

	NON-ALIN BOOMENTO				
*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)			
	U	Stanely Wolf and Richard N. Tauber, Silicon Processing For The VLSI Era, 2000, Lattice Press, Second Edition, pgs. 130-131 and 135-137			
	٧				
	w				
	×				

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).) Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.